AMENDMENTS TO THE DRAWINGS:

The attached sheet of one drawing includes a replacement drawing for Fig. 3. In replacement Fig. 3, the output from register 411C is connected to the data line that is connected to multiplexer 409.

REMARKS

In the Office Action[1], the Examiner objected to the drawings; rejected claims 1-6, 11, and 12 under 35 U.S.C. § 102(b) as being anticipated by Inoue et al. (U.S. Patent No. 5,982,380) ("*Inoue*"); rejected claims 1-6, 11, and 12 under 35 U.S.C. § 103(a) as being unpatentable over Negishi et al. (U.S. Patent No. 6,005,590) ("*Negishi*") in view of *Inoue*; rejected claims 7 and 8 under 35 U.S.C. § 103(a) as being unpatentable over *Negishi*, in view of *Inoue*, and further in view of Koss et al. (U.S. Patent No. 5,720,019) ("*Koss*"); and rejected claims 9 and 10 under 35 U.S.C. § 103(a) as being unpatentable over *Negishi*, in view of *Inoue*, and further in view of Oliver et al. (U.S. Patent No. 5,313,610) ("*Oliver*").

Claims 1 and 5 have been amended. Claims 1-12 remain pending.

Regarding the objection to the drawings, Applicants have attached a replacement drawing for figure 3. The replacement drawing depicts the output from register 411C connected to the data line that is connected to multiplexer 409 . Therefore, Applicants respectfully request reconsideration and withdrawal of the objection to the drawings.

Applicants respectfully traverse the rejection of claims 1-6, 11, and 12 under 35 U.S.C. § 102(b) as anticipated by *Inoue*. In order to properly establish that *Inoue* anticipates Applicants' claimed invention under 35 U.S.C. § 102, each and every element of each of the claims in issue must be found, either expressly described or under principles of inherency, in that single reference. Furthermore, "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." *See*

[1] The Office Action contains a number of statements reflecting characterizations of the related art and the claims. Regardless of whether any such statement is identified herein, Applicants decline to automatically subscribe to any statement or characterization in the Office Action.

M.P.E.P. § 2131, quoting *Richardson v. Suzuki Motor Co.*, 868 F.2d 1126, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989).

Independent claim 1 recites a clipping device including, for example:

> a current clip register for shifting the clip codes generated at said clip code generation circuit;
>
> clip registers cascade connected to an output of said current clip register for replacing the held data with the clip codes held by the register of a previous stage;
>
> . . .
>
> wherein,
>
> the current clip register includes a first clip register and corresponding first multiplexer, a second clip register and corresponding second multiplexer, and a third clip register and corresponding third multiplexer,
>
> the first multiplexer selects a clip code CLPC or a parameter for initialization from the clip code generation circuit and outputs the selection to a lower 2 bits of the first register,
>
> the second multiplexer selects the output of the first register or logic 0 and outputs the selection to a middle 2 bits of the second register, and
>
> the third multiplexer selects the output of the second register or logic 0 and outputs the selection to an upper 2 bits of the third register.

(emphasis added). *Inoue* does not teach or suggest at the least the current clip register of claim 1.

Inoue discloses a "clipping device for presenting an object to be displayed in a display area" (col. 2, lines 19-20). The Examiner asserts that register 23 corresponds to the claimed "current clip register" and latches 251-253 or 254-256 correspond to the claimed "clip registers cascade connected" (Office Action at page 14). Applicants respectfully disagree.

Register 23 has six registers 231 to 236, and the registers 231, 233 and 235 receive the output S and the registers 232, 234 and 236 receive the output L (col. 5, lines 35-37). According to a first embodiment, depicted in Fig. 4, registers 231-236

output values to a 6-input AND gate 24, which "outputs a logical product of the values in registers 231 to 236 as a judgment signal M1" (col. 6, lines 25-26). According to a third embodiment, depicted in Fig. 8, registers 231-236 output values to a 6-bit latch 254.

In *Inoue*, register 23, which includes registers 231-236, outputs values to AND gate 24 or 6-bit latch 254. Register 23 does not shift clip codes. On the contrary, any shifting that may occur in *Inoue* occurs with latches 251-253 or 254-256 as shown in Fig. 6 and Fig. 8, respectively. Therefore, *Inoue* does not teach or suggest the claimed "current clip register for shifting the clip codes generated at said clip code generation circuit," as recited in claim 1.

In addition, there is no teaching in *Inoue* that register 23 includes a first, second, and third multiplexer. Even assuming that multiplexers may exist, which is not disclosed in *Inoue* and Applicants do not concede, *Inoue* does not teach or suggest, "the first multiplexer selects a clip code CLPC or a parameter for initialization from the clip code generation circuit and outputs the selection to a lower 2 bits of the first register, the second multiplexer selects the output of the first register or logic 0 and outputs the selection to a middle 2 bits of the second register, and the third multiplexer selects the output of the second register or logic 0 and outputs the selection to an upper 2 bits of the third register," as further recited in claim 1.

Accordingly, *Inoue* cannot anticipate claim 1. Thus, claim 1 is allowable for at least these reasons and claims 2-4 are also allowable at least due to their depending from claim 1. Independent claim 5 and dependent claims 6, 11, and 12, while of different scope, recite limitations similar to those of claim 1 and are thus allowable over *Inoue* for at least the same reasons discussed above in regard to claim 1.

Applicants respectfully traverse the rejection of claims 1-6, 11, and 12 under 35 U.S.C. § 103(a). The prior art cited by the Examiner, *Negishi* in view of *Inoue*, does not teach or suggest each and every element of independent claim 1. A *prima facie* case of obviousness has, therefore, not been established.

The Examiner asserts that clip registers 304-306 of *Negishi* correspond to the claimed "current clip register" (Office Action at page 17). The Examiner also appears to assert that clip code register 308 corresponds to the claimed "clip registers cascade connected" (Office Action at page 18). Applicants respectfully disagree.

In *Negishi*, clip codes are supplied to shift registers 304, 305, and 306 (col. 8, lines 48-50 and Fig. 3). "The data in the shift registers 304, 305, and 306 are loaded to both the clip state code generator 307 and the clip code register 308" (col. 8, lines 53-55). "After the shift registers 304, 305, and 306 shift their fields, the generated clip codes for the second vertex are loaded to the respective shift registers 304, 305, and 306, and the clip state code 308 generates a clip state code" (col. 9, lines 30-34). Shift registers 304, 305, and 306 have parallel outputs connected to clip code register 308.

Negishi does not disclose the claimed "current clip register" that includes a "first multiplexer," "second multiplexer," and "third multiplexer." Therefore, *Negishi* does not teach or suggest, "the first multiplexer selects a clip code CLPC or a parameter for initialization from the clip code generation circuit and outputs the selection to a lower 2 bits of the first register, the second multiplexer selects the output of the first register or logic 0 and outputs the selection to a middle 2 bits of the second register, and the third multiplexer selects the output of the second register or logic 0 and outputs the selection to an upper 2 bits of the third register," as recited in claim 1.

In addition to the above deficiencies, clip code register 308 does not correspond to the claimed "clip registers cascade connected" at least because clip code register 308 is a single register, and there is no teaching or suggestion in *Negishi* of more than one clip code register 308. Therefore, *Negishi* also does not teach or suggest the claimed "clip registers cascade connected to an output of said current clip register for replacing the held data with the clip codes held by the register of a previous stage," as recited in claim 1.

Inoue does not cure the deficiencies of *Negishi*. As previously stated, *Inoue* does not teach or suggest the claimed "current clip register for shifting the clip codes generated at said clip code generation circuit," and "the first multiplexer selects a clip code CLPC or a parameter for initialization from the clip code generation circuit and outputs the selection to a lower 2 bits of the first register, the second multiplexer selects the output of the first register or logic 0 and outputs the selection to a middle 2 bits of the second register, and the third multiplexer selects the output of the second register or logic 0 and outputs the selection to an upper 2 bits of the third register," as recited in claim 1.

Accordingly, *Negishi* and *Inoue* fail to establish a *prima facie* case of obviousness with respect to claim 1, at least because the references fail to teach each and every element of the claim. Claims 2-4 depend from claim 1 and are thus also allowable over *Negishi* and *Inoue*, for at least the same reasons as claim 1.

Independent claim 5, though of different scope from claim 1, is allowable for at least the same reasons as claim 1. Claims 6, 11, and 12 depend from claim 5 and are thus also allowable over *Negishi* and *Inoue*, for at least the same reasons as claim 5.

Applicants respectfully traverse the rejection of claims 7 and 8, dependent from claim 5. The Examiner relies on *Koss* for allegedly teaching a control circuit that "generates a vertex ready flag indicating that the vertexes' worth of clip codes of said primitive are ready at the time of execution of the replacement instruction" (Office Action at page 33). Even assuming this assertion is true, *Koss* fails to cure the deficiencies of *Negishi* and *Inoue* discussed above. *Koss* discloses vertex clip code shift registers 220, 244, 246, and 248 (Fig. 4). First vertex clip code shift register 220 includes a series of six single-bit memory cells 232 (323 in Figure 4), 234, 236, 238, 240, and 242 (col. 9, lines 52-55).

Koss does not teach or suggest the claimed "current clip register for a shifting the clip codes generated at said clip code generation circuit in accordance with a control signal," and "the first multiplexer selects a clip code CLPC or a parameter for initialization from the clip code generation circuit and outputs the selection to a lower 2 bits of the first register, the second multiplexer selects the output of the first register or logic 0 and outputs the selection to a middle 2 bits of the second register, and the third multiplexer selects the output of the second register or logic 0 and outputs the selection to an upper 2 bits of the third register," as recited in claim 5. Therefore, claims 7 and 8 are also allowable over *Negishi*, *Inoue*, and *Koss* for at least the same reasons as claim 5.

Applicants respectfully traverse the rejection of claims 9 and 10, dependent from claim 5. Although the Examiner cites *Oliver* in the rejection of dependent claims 9 and 10, Applicants respectfully assert that *Oliver* fails to cure the deficiencies of *Negishi* and

Inoue discussed above. Therefore, claims 9 and 10 are also allowable over *Negishi*, *Inoue*, and *Oliver* for at least the same reasons as claim 5.

In view of the foregoing amendments and remarks, Applicants respectfully request reconsideration of the application and withdrawal of the rejections. Pending claims 1-12 are in condition for allowance, and Applicants request a favorable action.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: May 22, 2007

By: _____
Michael R. Kelly
Reg. No. 33,921

Attachments:
(1) Replacement Drawing Sheet (1 page)